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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,639	12/05/2003	Gary L. Swoboda	TI-34663	1122

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EXAMINER	
SCHELL, JOSEPH O	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,639	SWOBODA ET AL.	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 10-14* is/are allowed.

6)☒ Claim(s) *8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-14 have been examined.

Claims 8-9 have been rejected.

Claims 1-7 and 10-14 are allowable pending the resolution of claim objections.

Claim Objections

1. The claims are objected to for the following informalities:

Claim 1 line 13 ends with an oddly fragmented "the periodic signals" which should probably be removed.

Claim 1 line 16 should read "generating **a** reset marker..."

Claim 1 lines 18-19 and claim 5 lines 9-10 recite the limitation "the program execution." This term lacks antecedent basis and should either be changed to the program counter trace stream or defined within the claim.

Claim 2 lines 1-2 should read "wherein the **reset** marker signal group includes..."

Claims 8 and 9, lines 3-4 should read "a marker signal group included in **the plurality of trace streams**" to tie the environment limitations to the preamble.

Claim 10 line 2 should read "**a** program counter trace generation apparatus..."

Claim 10 line 5 should read "decoder unit responsive to a **reset** signal..."

Allowable Subject Matter

2. Claims 1-7 and 10-14 are allowable.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 1, within the entirety of the claim, the examiner deems the novel limitation to be the synchronization apparatus applying periodic signals to the timing trace and the program counter trace. Regarding claim 5, within the entirety of the claim, the examiner deems the novel limitation to be the inclusion of a reset marker in the program counter trace stream and relating the marker to the timing trace and the program execution. Regarding claim 10, within the entirety of the claim, the examiner deems the novel limitation to be the storage of a reset signal identification for conveyance to a host processor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mann (US Patent 6,314,530) in view of Orfali (US patent 7,039,834) and Kaneko (US Patent 5,440,700).

Mann ('530) discloses in a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit (see abstract and the

setup as shown in figure 1), a marker signal group included in a trace signal stream, the marker signal group comprising:

indicia of the occurrence of a reset signal (about the middle of the abstract, the tracing occurs on start or restart of an executable thread).

Mann ('530) does not disclose the environment wherein the marker signal group comprises indicia of the relationship of the occurrence of the reset signal to the target processor clock; and indicia of the relationship of the occurrence of the reset signal to the target processor program execution.

Orfali ('834) teaches a system that associates timestamps with events on a bus trace (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the tracing system performed by Mann ('530) such that a timestamp is associated with a traced event. This modification would have been obvious because when tracing multiprocessor systems it is important to know when a traced event occurred for a particular processor (Orfali ('834) column 2 line 62 through column 3 line 6).

Kaneko ('700) teaches a system that outputs, among other things, a program counter value to an external device when executing a halt instruction (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the tracing system performed by Mann ('530) such that a program counter value is associated with a traced event. This modification would have been obvious because the program counter address is extremely useful for debugging purposes (Kaneko ('700) column 2 lines 32-34).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mann (US Patent 6,314,530) in view of Why All Reset Signals are Active Low, Orfali (US patent 7,039,834) and Kaneko (US Patent 5,440,700)

As per claim 9, this claim expresses the same limitations as claim 8, save that the signal group comprises indicia of the removal of a reset signal instead of the occurrence of a reset signal.

Mann ('530) discloses in a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit (see abstract and the setup as shown in figure 1), a marker signal group included in a trace signal stream, the marker signal group comprising:

indicia of the occurrence of a reset signal (about the middle of the abstract, the tracing occurs on start or restart of an executable thread).

Mann ('530) does not expressly disclose the environment wherein the marker signal includes indicia of the removal of a reset signal instead of the occurrence of a reset.

"Why All Reset Signals are Active Low" talks about the use of active low signaling for reset signals.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the trace signal stream disclosed by Mann ('530) such that it includes indicia of the removal of a reset signal, or the occurrence of an active low reset signal. This modification would have been obvious because CMOS logic is less sensitive to noise occurring in active low signals ("Why All Reset Signals are Active Low," first paragraph).

Mann ('530) in view of "Why All Reset Signals are Active Low" does not disclose the environment wherein the marker signal group comprises indicia of the relationship of the occurrence of the reset signal to the target processor clock; and indicia of the relationship of the occurrence of the reset signal to the target processor program execution.

Orfali ('834) teaches a system that associates timestamps with events on a bus trace (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the tracing system performed by Mann ('530) in view of "Why All Reset Signals are Active Low" such that a timestamp is associated with a traced event. This modification would have been obvious because when tracing multiprocessor systems it is important to know when a traced event occurred for a particular processor (Orfali ('834) column 2 line 62 through column 3 line 6).

Kaneko ('700) teaches a system that outputs, among other things, a program counter value to an external device when executing a halt instruction (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the tracing system performed by Mann ('530) in view of "Why All Reset Signals are Active Low" such that a program counter value is associated with a traced event. This modification would have been obvious because the program counter address is extremely useful for debugging purposes (Kaneko ('700) column 2 lines 32-34).

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Hervin ('560) teaches a system that runs an SMI to output a processor state to a trace system before restarting, Floyd ('403) teaches a trace system that reads start codes, stop addresses, and time

stamps to reconstruct trace sequences, and Agarwala ('197) teaches a tracing system that continues tracing through a target processor reset event.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER